USB to Quad Serial Ports Chip CH9104

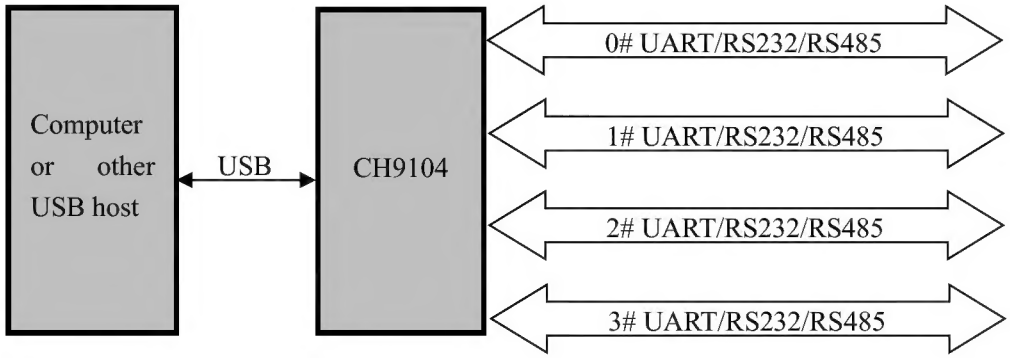
Datasheet

Version: 1

http://wch.cn

1. Overview

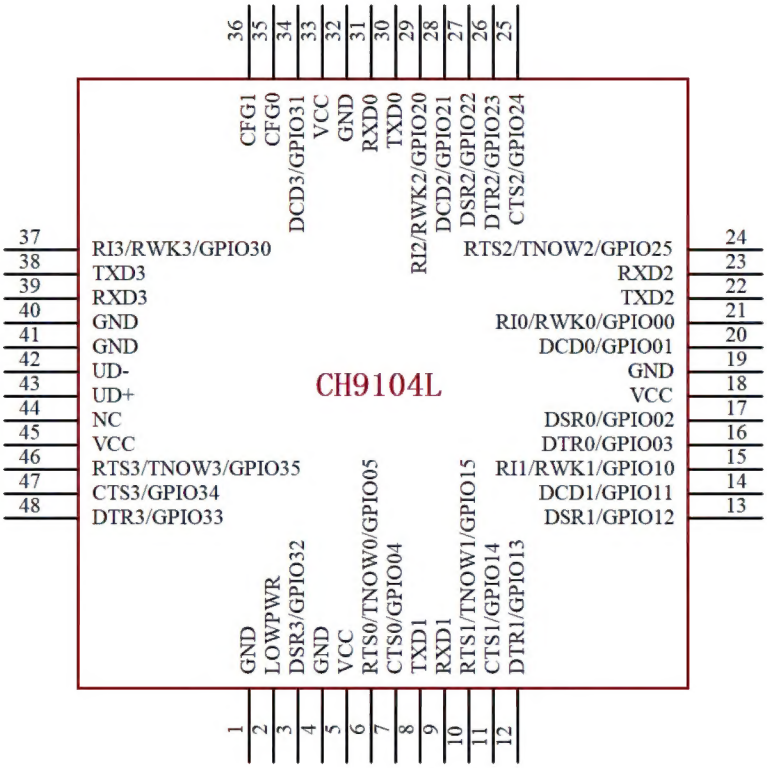
CH9104 is a USB bus converter chip which convers USB to quad asynchronous serial ports UART0/1/2/3 for extending asynchronous serial ports for computer, or upgrade normal serial devices or MCUs directly to USB bus.



2. Features

- Full-speed USB device interface, USB 2.0 compatible.
- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional serial port via USB.
- Original UART applications are totally compatible without any modification in Windows operating systems.
- Supports free installation OS which built-in CDC driver or multi-functional high-speed VCP vendor driver.
- Hardware full duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate from 1200bps to 6Mbps.
- Supports 8 data bits, supports odd, even, and no parity.
- Built-in 2048-byte RX-FIFO and 1024-byte TX-FIFO for each serial port.
- Supports common MODEM signals RTS, DTR, DCD, RI, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW which supports RS485 switching.
- Supports up to 24-channel GPIO input and output function.
- Supports RS232/RS485/RS422 interface, through external voltage conversion chip.
- Built-in EEPROM, used to configure the chip of VID, PID, maximum current value, vendor and product information string, etc.
- Supports only 3.3V power supply voltage.
- RoHS compliant LQFP48 lead-free package.

3. Package



Package	Body size	Lead pitch		Description	Part No.
LQFP48	7*7mm	0.5mm	19.7mil	Standard LQFP 48-pin patch	CH9104L

Note: USB transceiver of CH9104 is designed in accordance with the USB2.0 full built-in design, UD+ and UD- pins cannot connect with resistor in series, otherwise, it will affect the signal quality.

4. Pin definitions

Pin No.	Pin Name	Pin Type	Pin Description
5,18,33,45	VCC	POWER	Power supply voltage input, requires an external decoupling capacitor
1,4,19, 32,40,41	GND	POWER	Ground, connected to ground of USB bus directly
43	UD+	USB signal	Connect to USB D+ signal directly, do not connect resistor in series
42	UD-	USB signal	Connect to USB D- signal directly, do not connect resistor in series
30	TXD0	OUT	Transmit asynchronous data output of UART0, high when idle
31	RXD0	IN(FT)	Receive asynchronous data input of UART0, built-in pull-up resistor

21	RI0/ RWK0/ GPIO00	OUT/IN	MODEM input signal of UART0,ring indicator, active low; USB wake-up event detection input 0,active low, built-in pull-up resistor General GPIO00, used for IO input or output.
20	DCD0/ GPIO01	OUT/IN	MODEM input signal of UART0, data carrier detect, active low; General GPIO01, used for IO input or output.
17	DSR0/ GPIO02	OUT/IN	MODEM input signal of UART0, data set ready, active low; General GPIO02, used for IO input or output.
16	DTR0/ GPIO03	OUT/IN	MODEM output signal of UART0, data terminal ready, active low; General GPIO03, used for IO input or output. During power-on, if this pin detects an external pull-down resistor, then disable the configuration parameters in the internal EEPROM and enable chip default parameters
7	CTS0/ GPIO04	OUT/IN (FT)	MODEM input signal of UART0, clear to send, active low; General GPIO04，used for IO input or output.
6	RTS0/ TNOW0/ GPIO05	OUT/IN (FT)	MODEM output signal of UART0, request to send, active low; The RS485 transmit and receive control pin of UART0; General GPIO05, used for IO input or output. During power-on, if this pin detects an external pull-down resistor, then switch to TNOW function, otherwise it is RTS function;
8	TXD1	OUT	Transmit asynchronous data output of UART1, high when idle
9	RXD1	IN	Receive asynchronous data input of UART1, built-in pull-up resistor
15	RI1/ RWK1/ GPIO10	OUT/IN	MODEM input signal of UART1, ring indicator, active low; USB wake-up event detection input 1, active low, built-in pull-up resistor General GPIO10, used for IO input or output.
14	DCD1/ GPIO11	OUT/IN	MODEM input signal of UART1, data carrier detect, active low; General GPIO11, used for IO input or output.
13	DSR1/ GPIO12	OUT/IN	MODEM input signal of UART1, data set ready, active low; General GPIO12, used for IO input or output.
12	DTR1/ GPIO13	OUT/IN (FT)	MODEM output signal of UART1, data terminal ready, active low; General GPIO13, used for IO input or output. During power-on, if this pin detects an external pull-down resistor, then all UARTs are enabled hardware flow control function;

11	CTS1/ GPIO14	OUT/IN (FT)	MODEM input signal of UART1, clear to send, active low; General GPIO14, used for IO input or output.
10	RTS1/ TNOW1/ GPIO15	OUT/IN (FT)	MODEM output signal of UART1, request to send, active low; The RS485 transmit and receive control pin of UART1; General GPIO15, used for IO input or output. During power-on, if this pin detects an external pull-down resistor, then switch to TNOW function, otherwise it is RTS function;
22	TXD2	OUT	Transmit asynchronous data output of UART2, high when idle
23	RXD2	IN	Receive asynchronous data input of UART2, built-in pull-up resistor
29	RI2/ RWK2/ GPIO20	OUT/IN (FT)	MODEM input signal of UART2, ring indicator, active low; USB wake-up event detection input 2, active low, built-in pull-up resistor General GPIO20, used for IO input or output.
28	DCD2/ GPIO21	OUT/IN	MODEM input signal of UART2, data carrier detect, active low; General GPIO21, used for IO input or output.
27	DSR2/ GPIO22	OUT/IN	MODEM input signal of UART2, data set ready, active low; General GPIO22, used for IO input or output.
26	DTR2/ GPIO23	OUT/IN	MODEM output signal of UART2, data terminal ready, active low; General GPIO23, used for IO input or output.
25	CTS2/ GPIO24	OUT/IN	MODEM input signal of UART2, clear to send, active low; General GPIO24, used for IO input or output.
24	RTS2/ TNOW2/ GPIO25	OUT/IN	MODEM output signal of UART2, requests to sent, active low; The RS485 transmit and receive control pin of UART2; General GPIO25, used for IO input or output. During power-on, if this pin detects an external pull-down resistor, then switch to TNOW function, otherwise it is RTS function;
38	TXD3	OUT	Transmit asynchronous data output of UART3, high when idle
39	RXD3	IN (FT)	Receive asynchronous data input of UART3, built-in pull-up resistor.
37	RI3/ RWK3/ GPIO30	OUT/IN (FT)	MODEM input signal of UART3, ring indicator, active low; USB wake-up event detection input 3, active low, built-in pull-up resistor. General GPIO30, used for IO input or output.
34	DCD3/	OUT/IN	MODEM input signal of UART3, data carrier detect, active low;

	GPIO31	(FT)	General GPIO31, used for IO input or output.
3	DSR3/ GPIO32	OUT/IN	MODEM input signal of UART3, data set ready, active low; General GPIO32, used for IO input or output.
48	DTR3/ GPIO33	OUT/IN (FT)	MODEM output signal of UART3, data terminal ready, active low; General GPIO33, used for IO input or output.
47	CTS3/ GPIO34	OUT/IN (FT)	MODEM input signal of UART3, clear to send, active low; General GPIO34, used for IO input or output.
46	RTS3/ TNOW3/ GPIO35	OUT/IN (FT)	MODEM output signal of UART3, request to send, active low; The RS485 transmit and receive control pin of UART3; General GPIO35，used for IO input or output. During power-on, if this pin detects an external pull-down resistor, then switch to TNOW function, otherwise it is RTS function;
2	LOWPWR	OUT/IN (FT)	USB suspend status output, active low, output high level in normal working state, output low level after suspended; During power-on, the output polarity of the pin will be switched if an external pull-down resistor is detected on the pin.
35	CFG0	IN (FT)	Remote wake-up and USB power mode configuration pin 0
36	CFG1	IN (FT)	Remote wake-up and USB power mode configuration pin 1
44	NC	/	No connection, must be suspended

Note: CH9104L chip: FT means the pin can tolerate 5V voltage when used as input.

5. Functional description

5.1. General description

CH9104 supports 3V supply voltage, the power supply pins should be externally connected to an external power decoupling capacitor of about 0.1uF to ground respectively.

CH9104 has a built-in power-on reset circuit, and a clock circuit required for chip operation.

CH9104 has built-in all the peripheral circuits required by the USB bus, including the embedded USB controller and USB-PHY, the series matching resistor of the USB signal line, and the 1.5K pull-up resistor required for the device. The UD+ and UD- pins can be connected directly to a PC or other USB host. If the chip is connected in series with an insurance resistor, inductor or ESD protection device for chip safety, then the AC/DC equivalent series resistor should be within 5Ω.

5.2. UART

CH9104 chip provides 4 groups of asynchronous serial ports UART0/1/2/3, each group includes TXD, RXD,

RI, DSR, DCD, DTR, CTS and RTS pins, which can realize 3-line UART, 5-line UART or 9-line UART communication.

In UART mode, the pins of CH9104 chip include: data transfer pins, MODEM contact signal pins and auxiliary pins.

Data transfer pins include: TXD0, RXD0, TXD1, RXD1, TXD2, RXD2, TXD3 and RXD3. RXDx is high when UART input is idle. TXDx is high when UART output is idle.

MODEM contact signal pins include: CTS0, RTS0, DTR0, DCD0, RI0, DSR0, CTS1, RTS1, DTR1, DCD1, RI1, DSR1, CTS2, RTS2, DTR2, DCD2, RI2, DSR2, CTS3, RTS3, DTR3, DCD3, RI3, DSR3.

Auxiliary pins include: TNOW0, TNOW1, TNOW2, TNOW3, LOWPWR, CFG0 and CFG1, etc. TNOWx is the RS485 transmit and receive control pin corresponding to the UART, this pin is multiplexed with the RTSx pin, and the default is the RTSx function. If an external pull-down resistor is detected on this pin during power-on, it will switch to the TNOW function. The DTR1 pin of the CH9104 chip can be multiplexed as the hardware automatic flow control configuration pin, the chip detects the level status of this pin at power-on, when it is suspended or the input is high level, disabling hardware flow control; When the input is low level then enable hardware flow control. LOWPWR pin is the USB suspend state output, active low, output high level in normal working state, output low level after suspended. If an external pull-down resistor is detected on this pin during power-on, the output polarity of this pin is switched. CFG0 and CFG1 pins are remote wake-up and USB power mode configuration pins.

Each UART of the CH9104 chip has a built-in independent transmit and receive buffer and supports simplex, half-duplex or full-duplex asynchronous serial communication.

The serial data of UART0/1/2/3 includes 1 low level start bit, 8 data bits, 1 / 2 high level stop bits, and supports no/odd/even parity. CH9104 supports common communication baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M, 3M, 4M, 5M, 6M etc.

All 4 UARTs of the CH9104 chip support CTSx and RTSx hardware auto-flow control, which can be configured via the DTR1 pin to be enabled at the same time or disabled at the same time (default), or independently via the VCP vendor driver. If enabled, UART will continue to send the next data only when CTSx input is valid (active low), otherwise the UART transmission is paused; when the receive buffer is empty, UART will automatically set RTSx to be valid (active low), it will automatically invalidate RTSx pin until the data in the receive buffer is nearly full, and RTSx will be valid again when the buffer is empty. While using hardware automatic flow control, CTSx pin of CH9104 should connect to RTSx of the counterpart, and RTSx of CH9104 should connect to CTSx of the counterpart.

The allowable baud rate error of the CH9104 UART receive signal is not more than 2%, and the baud rate error of UART transmit signal is less than 1.5%.

In the Windows OS, CH9104 supports the CDC class drivers that come with the system, and can also install high speed VCP vendor driver, it can also emulate standard UART, so most UART applications are fully compatible and usually do not require any modification. Support up to 24-channel GPIO input and output control function in VCP vendor driver mode.

CH9104 can be used to upgrade the original UART peripheral devices, or expand extra UART for computers via USB bus. Further interfaces such as RS232, RS485, RS422 can be provided through the addition of level conversion devices.

5.3. Parameter configuration

In larger batch applications, the CH9104's vendor identification code (VID), product identification code (PID) and product information can be customized.

In less batch applications, parameters can be configured using the built-in EEPROM. after installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, users can be flexibly configure the vendor identification code (VID), product identification code (PID), maximum current value, BCD version number, vendor information and product information string descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

Critical state or exceeding maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-40	105	℃
VCC	Supply voltage(VCC connects to power, GND connects to ground)	-0.3	4.0	V
VUSB	USB signal voltage	-0.5	3.8	V
VIO5V	Withstand 5V on UART pins	-0.5	5.6	V
VUART	Voltage on UART and other pins	-0.5	VCC+0.3	V

6.2. Electrical characteristics

Test conditions: TA=25℃, VCC=3.3V, exclude USB pin

Name	Parameter Description	Min	Typ	Max	Unit
VCC	Supply voltage(VCC power supply, GND connects to ground)	3.0	3.3	3.6	V
ICC	Operating supply current	12	18	24	mA
ISLP	Supply current (USB suspend)	200	450	600	uA
VIL	Low level input voltage	0	/	0.8	V
VIH	High level input voltage	2.0	/	VCC	V
VIH5	High level input voltage withstanding 5V pin	2.0	/	5.0	V
VOL	Low level output voltage, 8mA sunk current	/	/	0.4	V
VOH	High level output voltage, 8mA output current	VCC-0.4	/	/	V

RPU	Built-in pull-up equivalent resistor	30	40	60	KΩ
VPOR	Threshold voltage for power-up/power-down reset	1.9	2.2	2.5	V
VESD	ESD tolerance (HBM, Non-Contact)	2	/	/	KV

6.3. Timing parameters

Test conditions: TA=25°C, VCC=3.3V

Name	Parameter Description		Min	Typ	Max	Unit
FD	Error of internal clock (Equiproportional impact on baud rate)	TA=0°C～70°C	-1.5	0.8	1.5	%
		TA=-40°C～85°C	-2	1.5	2	%
TRSTD	Reset delay after power on or external reset input		15	30	45	mS
TSUSP	Detect USB automatic suspend time		3	5	9	mS
TWAKE	Wake-up completion time after chip sleep		0.3	0.5	4	mS

7. Application

7.1. USB to 4-channel TTL UART

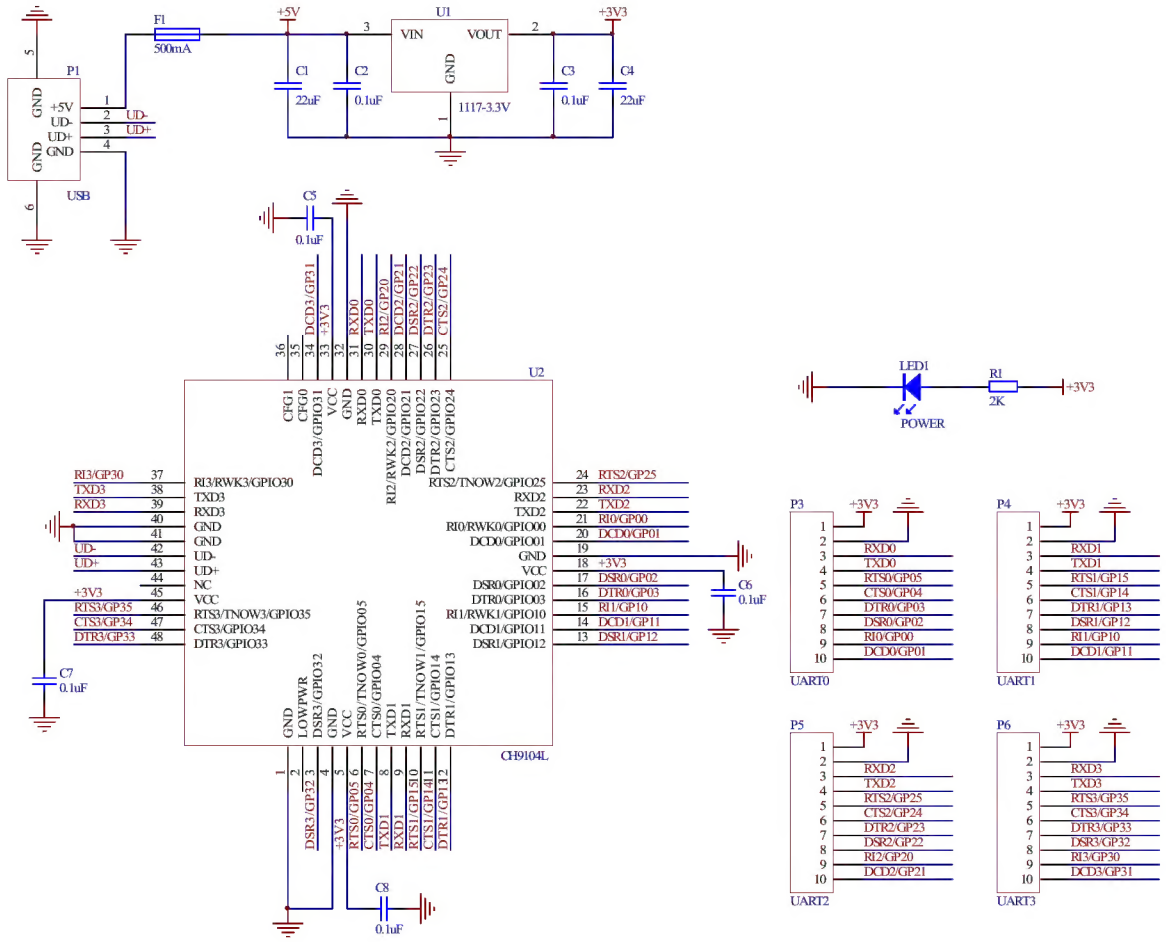
The figure below is the reference circuit diagram of the USB to quad TTL UART implemented by the CH9104 chip. The only signal lines in the diagram that need to be connected are RXDx, TXDx, and the common ground. Other signal lines such as CTSx, RTSx/TNOWx, DTRx, DSRx, RIx and DCDx are selected as needed and can be suspended when not needed.

P1 is USB port, the USB bus includes a pair of 5V power lines and a pair of data signal lines. Usually, the +5V power line is red, the ground line is black, the D+ signal line is green and the D- signal line is white. The USB bus can provide power supply current up to 500mA.

P3, P4, P5 and P6 are the TTL connection pins for each UART, including VCC, GND, RXDx, TXDx, RTSx, CTSx and TNOWx pins. TTL to RS232, RS485, RS422 and other signals can be converted by adding level conversion devices.

CH9104 chip supports 3.3V power supply voltage, each power supply pin should be connected to the external power supply decoupling capacitor with a capacity of about 0.1 uF. In the figure, C5, C6, C7 and C8 are the power supply decoupling capacitors.

It is recommended to add ESD protection devices for USB signal lines, ESD chip parasitic capacitance should be less than 2pF, such as CH412K.

It is recommended that the serial peripheral and CH9104 chip use the same power supply, otherwise the IO pin backflow current problem needs to be considered when the power is supplied separately.

When designing the PCB, pay attention to: the decoupling capacitors C5, C6, C7 and C8 should be as close as possible to the connected pins of CH9104; The D+ and D- signal lines of the USB port are wired close to parallel according to the high-speed USB specification to ensure the characteristic impedance, and surrounding the relevant components with ground lines or copper cladding can reduce signal interference from outside.